In the claims:

1. (Currently amended) A computer system comprising:

a processor;

a memory unit configured to store data used by the processor;

a memory control unit configured to manage data flowing into and out of the memory unit;

a circuit board comprising:

at least two layers formed in parallel to a surface of said circuit board,

a first signal line, formed on a first layer of the circuit board and connected between a first pin ~~connection~~ on the memory unit and the memory control unit; and

a second signal line also formed on the first layer of the circuit board and connected to the first pin ~~connection~~ on the memory unit, a first portion of the second signal line ~~substantially parallel~~ at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line substantially parallel ~~at an acute angle relative~~ to a second portion of the first signal line,

~~wherein the widths of the lines and the distance separating the lines are each substantially equal,~~ and

wherein said first layer defines a non-grounded gap between said first and second lines.

2. (Cancelled)

3. (Original) The system of claim 1, further comprising third and fourth signal lines, on a second layer of the circuit board, different than the first layer.

4. (Previously amended) The system of claim 1, wherein the first signal line and the portion of the second signal line that is routed substantially parallel to the first signal line have substantially equal widths.

5. (Previously amended) The system of claim 4, wherein the first signal line and the portion of the second signal line that is routed substantially parallel to the first signal line are separated by a distance substantially equal to said widths.

6. (Previously amended) The system of claim 5, wherein the widths of the lines and the distance separating the lines are each substantially equal to 5 mils.

7. (Previously amended) The system of claim 1, wherein the memory unit comprises a RAMBUS™ device.

8. (Currently amended) A method for use in routing signals between a memory unit and a memory control unit, the method comprising:

delivering a first signal over a first signal line on a first layer formed in parallel to a second layer on a surface of a multi-layer circuit board and connected between the memory control unit and a first pin on the memory unit;

delivering a second signal over a second signal line formed on the first layer of the circuit board and connected to the first pin ~~connection~~ of the memory unit, a first portion of the second signal line formed ~~substantially parallel~~ at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line formed ~~at an acute angle relative~~ substantially parallel to a second portion of the first signal line~~, wherein the first and second portions of the first and second signal lines are substantially equal in width~~; and

separating said first and second signal lines without a ground connection therebetween.

9. (Cancelled)

10. (Previously amended) The method of claim 8, further comprising delivering another signal to said memory control unit on another parallel layer of the circuit board over portions of the first and second signal lines that are not separated by any conductive traces.

11. (Previously amended) The method of claim 8, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that have substantially equal widths.

12. (Previously amended) The method of claim 11, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that are separated by a distance substantially equal to their widths.

13. (Previously amended) The method of claim 12, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that are substantially equal to 5 mils wide and that are separated by a distance substantially equal to 5 mils.

14. (Currently amended) A method for use in manufacturing a computer system, the method comprising:

forming at least two parallel layers on a surface of a circuit board, with first and second signal lines on a first ~~selected~~ layer of the board;

connecting a memory unit to the board such that a first pin ~~connection~~ on the memory unit connects to the first and second signal lines;

affixing a memory control unit to the board such that the memory control unit connects to at least the first signal line;

forming a first portion of the second signal line to be ~~substantially parallel~~ at an acute angle relative to a first portion of the first signal line; and

forming a second portion of the second signal line to be ~~at an acute angle relative~~ substantially parallel to a second portion of the first signal line

~~forming the first and second portions of the first and second signal lines substantially equal in width~~.

15. (Cancelled)

16. (Previously amended) The method of claim 14, further comprising forming the first and second signal lines such that no conductive trace lies between the first signal line and the

first portion of the second signal line that is routed substantially parallel to the first signal line.

17. (Previously amended) The method of claim 16, further comprising forming the first signal line and the first portion of the second signal line that is routed substantially parallel to the first signal line to have substantially equal widths.

18. (Previously amended) The method of claim 17, further comprising forming the first signal line and the first portion of the second signal line that is routed substantially parallel to the first signal line to be separated by a distance approximately equal to their widths.

19. (Previously amended) The method of claim 18, further comprising forming the signal lines such that the widths of the lines and the distance separating the lines are all substantially equal to 5 mils.

20. (Currently amended) A circuit board comprising at least two layers formed in parallel to a surface of said circuit board for use in a computer system comprising:

a memory unit;

a memory control unit; and

a data bus connecting the memory control unit to the memory unit and comprising:

a first signal line formed on a first layer of the circuit board and connected to the memory control unit and to a first pin ~~connection~~ on the memory unit; and

a second signal line formed on the first layer of the circuit board and also connected to the first pin connection on the memory ~~control~~ unit, a first portion of the second signal line ~~substantially parallel~~ at an acute angle relative to a first portion of the first signal line, a second portion of the second signal line ~~at an acute angle relative~~ substantially parallel to a second portion of the first signal line,

wherein the widths of the lines and the distance separating the lines are each substantially equal, and

wherein said first layer defines a non-grounded gap between said first and second lines.

21-22. (Canceled)

23. (New) The computer system of claim 1, wherein the memory unit comprises a memory repeater hub.

24. (New) The circuit board of claim 20, wherein the memory unit comprises a memory repeater hub. --